REMARKS

Claims 1-3, 5-13, and 15-21 are pending. The Examiner's reconsideration of the objections and rejections in view of the amendments and remarks is respectfully requested.

The Specification has been objected to for an informality. The Specification has been amended to clarify the language of page 12, line 4, wherein the word "queues" has been amended to "units". The Examiner's reconsideration of the objection is respectfully requested.

Claim 14 has been objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of the previous claim. Claim 14 has been cancelled.

Claim 19 has been objected to because of informalities. The Applicant's appreciate the Examiner's suggestions. Claim 19 has been amended accordingly. Reconsideration of the objection is respectfully requested.

Claim 21 has been objected to because of informalities. Claim 21 has been amended according to the Examiner's suggestions. Reconsideration of the objection is respectfully requested.

Claim 11 has been rejected under 35 USC 112, wherein the Examiner suggested that "the decoded instructions" in line 6 lacks sufficient antecedent basis. Claim 11 has been amended to clarify the limitation. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 1 and 5-9 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni (U.S. Patent No. 6,223,254) in view of Chan (U.S. Patent No. 5,317,745). The Examiner stated essentially that the combined teachings of Soni and Chan teach or suggest all the limitations of claims 1 and 5-9.

Claim 1 claims, *inter alia*, "de-gating a plurality of execution queues storing a plurality of

instructions of the first instruction form." Claim 1 has been amended to include the limitations of claim 4, rejected under 35 USC 103(a) as being unpatentable over Soni in view of Chan, and further in view of Johnson ("Superscalar Microprocessor Design," Prentice Hall, 1991).

Soni teaches a reservation station 50 receiving instructions from a parcel cache 52 and a decode unit 43 (see Figure 3). Soni does not teach or suggest "de-gating a plurality of execution queues storing a plurality of instructions of the first instruction form" a claimed in claim 1. Soni teaches a parcel cache issuing instructions to the reservation station (see col. 7, lines 27-30). The reservation station of Soni is used storing the instructions of both the parcel cache and instructions of the decode unit. Because the reservation station of Soni is used by both the parcel cache and the decode unit, there is no need to de-gate the reservation station. Therefore, Soni fails to teach or suggest, "de-gating a plurality of execution queues storing a plurality of instructions of the first instruction form" as claimed in claim 1.

Chan teaches a program counter apparatus for reducing latency times, having multiple program counter values stored in memory locations corresponding to alternative program counters (see Abstract and col. 2, lines 23-41). Chan does not teach or suggest that "de-gating a plurality of execution queues storing a plurality of instructions of the first instruction form" as claimed in claim 1. Chan teaches a memory used as a program counter (see col. 3, lines 31-36). Nowhere does Chan does not teach or suggest an execution queue, much less, de-gating an execution queue. Thus, Chan does not teach or suggest, "de-gating a plurality of execution queues storing a plurality of instructions of the first instruction form" as claimed in claim 1. Therefore, Chan fails to sure the deficiencies of Soni.

Johnson teaches designs for a central instruction window and in the alternative reservation stations (see page 133). Johnson does not teach or suggest "de-gating a plurality of execution

queues storing a plurality of instructions of the first instruction form" a claimed in claim 1. Johnson merely teaches differences and similarities between a central window and a reservation station. However, nowhere does Johnson teach or suggest, "de-gating a plurality of execution queues storing a plurality of instructions of the first instruction form" as claimed in claim 1. Therefore, Johnson fails to cure the deficiencies of Soni and Chan.

Further, the proposed modification would render the prior art invention unsatisfactory for its intended purpose. For example, de-gating the reservation station of Soni would halt all executions of instructions because both the parcel cache and the decode unit utilize the reservation station. Therefore, Applicants respectfully submit that there is no suggestion or motivation to make the proposed modification.

For at least the forgoing reasons, Applicants believe that the combined teachings of Soni, Chan, and Johnson fail to teach or suggest, "de-gating a plurality of execution queues storing a plurality of instructions of the first instruction form" a claimed in claim 1.

Claims 5-9 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 2 and 3 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Chan, as applied to claims 1 and 5-9, and further in view of Lavi (U.S. Patent No. 6,453,407). The Examiner stated essentially that the combined teachings of Soni, Chan and Lavi teach or suggest all the limitations of claims 2 and 3.

Claims 2 and 3 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. Reconsideration of the rejection is respectfully requested.

Claims 4 and 10 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Chan, as applied to claims 1 and 5-9, and further in view of Johnson ("Superscalar Microprocessor Design," Prentice Hall 1991). The Examiner stated essentially that the combined teachings of Soni, Chan and Johnson teach or suggest all the limitations of claims 4 and 10.

Claims 4 and 10 depend from claim 1. The dependent claims are believed to be allowable for at least the reasons given for claim 1. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 11-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Johnson. The Examiner stated essentially that the combined teachings of Soni and Johnson teach or suggest all the limitations of claims 11-19.

Claim 11 claims, *inter alia*, "a branch unit connected to an instruction fetch unit for the first instruction form and a sequencer for the second instruction form, wherein the sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units."

Respectfully, Applicants believed that the Examiner has used impermissible hindsight in suggesting that, "It would also have been obvious to one of ordinary skill in the art at the time of the invention to modify the processor by providing the instructions of the second form (decoded instructions) in the parcel cache directly to the execution units" (see Response to Arguments, page 12, point 59). Soni is completely devoid of any teaching or suggestion of how a processor might function without a reservation station. Likewise, Johnson fails to teach or suggest a modification by which a processor might operate without a central window or reservation station. Therefore, the combined teachings of Soni and Johnson fail to teach or suggest the modification

described in the Final Office Action at page 12, point 59.

Even assuming, arguendo, that the modifications suggested in the Final Office Action at page 12, point 59 can be made, the combined teachings of Soni and Johnson fail to teach or suggest all the limitations of claim 11.

Soni teaches a parcel cache for storing decoded instructions coupled to an instruction streaming buffer, a decoded instruction queue and a reservation station (see Abstract and Figure 3). Soni does not teach or suggest that a "sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in claim 11. Soni teaches that the reservation station is connected to the execution units (see for example, Figures 3 and 4, col. 5, line 65 to col. 6, line 5, col. 6, lines 20-22, col. 7, lines 27-30, and col. 9, lines 11-13). Soni fails to teach or suggest how to execute an instruction of the parcel cache without the reservation station. Thus, Soni does not teach or suggest that a "sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in claim 11. Therefore, Soni fails to teach or suggest all the limitations of claim 11.

Johnson teaches designs for a central instruction window and in the alternative reservation stations (see page 133). Johnson does not teach or suggest that a "sequencer controls a plurality of gates connected between a plurality of execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in claim 11. Johnson merely compares a central window and a reservation station. Johnson teaches that a reservation station corresponds to a functional unit (see page 134, line 17). However, nowhere does Johnson teach or suggest that a "sequencer controls a plurality of gates connected between a plurality of

execution queues for storing decoded instructions of the first instruction form and the plurality of execution units" as claimed in claim 11. Therefore, Johnson fails to cure the deficiencies of Soni.

Claims 12, 13, and 15-19 depend from claim 11. The dependent claims are believed to be allowable for at least the reasons given for claim 11. The Examiner's reconsideration of the rejection is respectfully requested.

Claims 20-21 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Soni in view of Johnson, and further in view of Lavi. The Examiner stated essentially that the combined teachings of Soni, Johnson and Lavi teach or suggest all the limitations of claims 20-21.

Claim 20 depends from claim 11. Claim 20 is believed to be allowable for at least the reasons given for claim 11.

Claim 21 claims, *inter alia*, "the sequencer, engaged by the branch unit, adapted to fetch the predecoded instructions and sequence the predecoded instructions of the second instruction form, wherein the sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates."

Soni teaches a parcel cache for storing decoded instructions coupled to an instruction streaming buffer, a decoded instruction queue and a reservation station (see Abstract and Figure 3). Soni does not teach or suggest that a "sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. Soni teaches that the reservation station is connected

to the execution units (see for example, Figures 3 and 4, col. 5, line 65 to col. 6, line 5, col. 6, lines 20-22, col. 7, lines 27-30, and col. 9, lines 11-13). Soni fails to teach or suggest how to execute an instruction of the parcel cache without the reservation station. Further, nowhere does Soni teach or suggest the use of gates anywhere in the described processor. Thus, Soni does not teach or suggest that a "sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. Therefore, Soni fails to teach or suggest all the limitations of claim 21.

Johnson teaches designs for a central instruction window and in the alternative reservation stations (see page 133). Johnson does not teach or suggest that a "sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" a claimed in claim 21. Johnson merely compares a central window and a reservation station. Johnson teaches that a reservation station corresponds to a functional unit (see page 134, line 17). Nowhere does Johnson teach or suggest structures other the a central window, reservation stations, or functional units, much less that a "sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. Therefore, Johnson fails to cure the deficiencies of Soni.

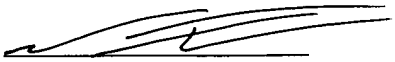
Lavi teaches a configurable long instruction word (CLIW) array having information about the operation to be performed and additional operands which need not be specified until execution state (see col. 13, lines 26-33). Lavi does not teach or suggest that a "sequencer is

connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. Lavi's array does not teach or suggest execution queues, much less a gate connected between a plurality of execution queues and the plurality of execution units, essentially as claimed in claim 21. Therefore, Lavi fails to cure the deficiencies of Soni and Johnson.

The combined teachings of Soni, Johnson and Lavi fail to teach or suggest that a "sequencer is connected to a plurality of gates connected between a plurality of execution queues adapted to store the decoded instructions of the first instruction form and the plurality of execution units, the sequencer further adapted to control the gates" as claimed in claim 21. The Examiner's reconsideration of the rejection is respectfully requested.

For the forgoing reasons, the application, including claims 1-3, 5-13, and 15-21, is believed to be in condition for allowance. Early and favorable reconsideration of the case is respectfully requested.

Respectfully submitted,



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